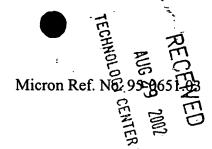
Docket No. 303.098US4 *WD* # 408120





Clean Version of Pending Claims

LOW ANGLE, LOW ENERGY PHYSICAL VAPOR DEPOSITION OF ALLOSS Applicant: Yong-Jun Hu

Serial No.: 09/826,661

Claims 48-54 and 71-107, as of August 19, 2002 (date of response to final office action filed).

- 48. A contact hole for a semiconductor device, comprising:
 - a bottom surface of a first material;
 - at least one vertical sidewall of a second material;
- a generally planar layer of a third material covering only the bottom surface, the third material having a graded stoichiometry between two different elements.
- 49. The contact hole of claim 48 where the hole has a high aspect ratio.
- 50. The contact hole of claim 48 where the first material is silicon.
- 51. The contact hole of claim 48 where the second material is an insulator.
- 52. The contact hole of claim 48 where the planar layer contacts the sidewalls.
- 53. The contact hole of claim 52 where the third material is substantially confined to the bottom of the hole.
- 54. The contact hole of claim 48/where the third material is a silicide.

71. In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:

a bottom surface having at least one generally planar layer of conductive material including at least two different constituent elements; and

a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator material.

- 72. The device of claim 71 where the planar layer contacts the lower end of the sidewall.
- 73. The device of claim 72 where the planar layer does not extend substantially up the sidewall from the bottom surface.
- 74. The device of claim 71 where the planar layer is an alloy or a composite.
- 75. The device of claim 71 where the planar layer includes a silicide.
- 76. The device of claim 75 where the planar layer includes a refractory metal.
- 77. In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:

a bottom surface having at least one bottom layer of conductive material including at least two different constituent elements and having a thickness variation less than about 50%; and

a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator material.

78. The device of claim 77 where the hole has a high aspect ratio.

- 79. The device of claim 78 where the aspect ratio is at least 4.
- 80. The device of claim 77 where the thickness variation is less than about 20%.
- 81. The device of claim 80 where the thickness variation is less than about 10%.
- 82. In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:
- a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator material; and
- a bottom surface having at least one generally planar bottom layer of conductive material having a graded stoichiometry between two different constituent elements in the bottom layer.
- 83. The device of claim 82 where the substrate is silicon and the insulator material is an oxide, a nitride, or a glass.
- 84. The device of claim 82 where the planar layer comprises multiple layers having mutually different stoichiometries.
- 85. The device of claim 82 where the conductive material includes a silicide of a metal.
- 86. The device of claim 85 where the metal is a refractory metal.
- 87. In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:
- a bottom surface having at least one generally planar bottom layer of a conductive material including at least two different constituent elements; and

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a vertical sidewall comprising the aforementioned layer of insulator material and being free of the conductive elements.

- 88. The device of claim 87 where the planar/layer contacts the lower end of the sidewall.
- 89. The device of claim 88 where the planar layer does not extend substantially up the sidewall from the bottom surface.
- 90. The device of claim 87 where the planar layer is an alloy or a composite.
- 91. The device of claim 87 where the planar layer includes a silicide.
- 92. The device of claim 91 where the planar layer includes a refractory metal.
- 93. In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:

a bottom surface having at/least one generally planar bottom layer of conductive material including a silicide of a metal,

a vertical sidewall comprising the aforementioned layer of insulator material, and being substantially free of the metal.

- 94. The device of claim 93 where the metal is a refractory metal.
- 95. The device of claim 93 where the insulator material is an oxide, a nitride, or a glass.
- 96. The device of claim 93 where the planar layer has a graded stoichiometry.

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- 97. The device of claim 96 where the planar layer comprises multiple layers having mutually different stoichiometries.
- 98. An integrated circuit, comprising:
 - a substrate;
- a layer of insulating material overlying the substrate and containing at least one contact hole having only that layer as a sidewall and having a bottom surface contacting the substrate; and
- at least one generally planar layer of conductive material including at least two different constituent elements covering the bottom surface of the hole.
- 99. The integrated circuit of claim 98 where the planar layer contacts the lower end of the sidewall.
- 100. The integrated circuit of claim 99 where the planar layer does not extend substantially up the sidewall from the bottom surface.
- 101. The integrated circuit of claim 98 where the planar layer is an alloy or a composite.
- 102. The integrated circuit of claim 98 where the planar layer includes a silicide.
- 103. The integrated circuit of claim 102 where the planar layer includes a refractory metal.
- 104. An integrated circuit, comprising:
 - a substrate;
- a layer of insulating material overlying the substrate and containing at least one contact hole having only that layer as a sidewall and having a bottom surface contacting the substrate;

and

at least one generally planar layer of conductive material covering the bottom surface, the planar layer including a silicide of a metal, the metal being substantially entirely confined to the bottom surface in the hole.

- 105. The integrated circuit of claim 104 where the planar layer contacts the lower end of the sidewall.
- 106. The integrated circuit of claim 104 where the planar layer has a graded stoichiometry.
- 107. The integrated circuit of claim 106 where the planar layer comprises multiple layers having mutually different stoichiometries.